Amendments to the Claims

- 1. (CURRENTLY AMENDED) A data converter comprising a sigma delta modulator intended to operate at a specific sample frequency $\{f_s\}$ -said sigma delta modulator comprising in a feedback loop a comparator $\{G\}$, a discrete-time low-pass filter $\{FD\}$ -and a quantizer $\{Q\}$ -in that order, in which the comparator $\{G\}$ -is arranged to compare the output of the quantizer with the input signal $\{U\}$ -to be converted, characterized in that, for decreasing the idle oscillation frequency of the sigma delta modulator, the discrete-time low-pass filter is arranged to have a 180° phase delay with positive group delay at a frequency that is at least four times lower than the sample frequency $\{f_s\}$.
- 2. (CURRENTLY AMENDED) A data converter as claimed in claim 1 characterized in that the transfer function of the discrete-time low-pass filter (FD) comprises, in its complex z-plane, a plurality of poles at or close to the point (1;0) of the unit circle of said plane and an additional pole on the positive real axis of said plane at a value between 0.20 and 0.92 for decreasing the idle oscillation frequency of the sigma delta modulator.
- 3. (CURRENTLY AMENDED) A data converter as claimed in claim 2 characterized in that the transfer function of the discrete-time low-pass filter (FD)-has a number of poles that exceeds the number of zeros of said discrete-time low-pass filter by at least 2.
- 4. (CURRENTLY AMENDED) A data converter as claimed in claim 3 characterized in that the discrete-time low-pass filter (FD)-comprises a cascade of integrators $(I_1 \text{ to } I_6)$, summing means (AD) to sum the output of said integrators through coefficient multipliers $(C_1 \text{ to } C_6)$ -to constitute the output of the discrete-time low-pass filter and a single order low-pass filter section (L) positioned in series with the first of the integrators of said cascade for producing said additional pole on the real axis of the complex z-plane.